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Reply to Office Action of 09/25/03

Amendments to the Claims:

This listing will replace all prior versions, and listing, of claims in the application.

Claims 1-12: (cancelled).

13. (currently amended) A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active ~~surface~~ region ~~[[as]]~~ of said substrate as defined by regions of Shallow Trench Isolation provided in ~~the surface of~~ ~~the~~ said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly ~~[[Doper]]~~ Doped Diffusion regions having been provided in ~~the surface of~~ said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over ~~the surface of~~ said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

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depositing a thin layer of salicide material over ~~the surface of~~ said substrate, including ~~the surface of~~ said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

performing a first anneal, forming salicided layers comprising reacted salicide material over ~~the surface of~~ said source and drain implants;

first removing un-reacted salicide material from ~~the surface of~~ said substrate;

depositing an isolation film over ~~the surface of~~ said substrate, including ~~the surface of~~ said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of filler material over ~~the surface of~~ said isolation film to a thickness such that ~~the surface of~~ said layer of filler material extends above ~~the surface of~~ said isolation film even where said isolation film overlays ~~the surface of~~ said at least one gate electrode, said depositing a layer of filler material over said layer of etch stop material comprises depositing a layer of photoresist;

polishing ~~the surface of~~ said layer of filler material and said layer of isolation film down to ~~the surface of~~ said layer of boronitride of said at least one gate electrode, using said

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layer of boronitride as a stop for said process of polishing,

advantageously using a polishing rate of filler material that is larger than a polishing rate of boronitride, said layer of boronitride providing a save stop for said polishing ~~the surface of~~ the layer of filler material and the layer of isolation film, thereby further preventing corrosion of ~~the surface of~~ said at least one gate electrode;

removing said layer of boronitride from said at least one gate electrode, exposing ~~the surface of~~ said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of salicide material over ~~the surface of~~ said polished layer of filler material, including the exposed surface of said layer of polysilicon;

performing a second anneal of said deposited thick layer of salicide material, a layer of reacted salicide material overlying said layer of polysilicon of said at least one gate electrode;

second removing un-reacted salicide material from ~~the surface of~~ said layer of dielectric;

performing a third anneal, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.

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14. (currently amended) The method of claim 13 wherein said depositing a thin layer of salicide material over ~~the surface of~~ said substrate comprises depositing a thin layer of Ti/TiN, deposited to a thickness between about 100 and 500 Angstrom ~~and more preferably to a thickness of about 300 Angstrom.~~

15. (currently amended) The method of claim 13 wherein said first anneal is a low temperature anneal performed by rapid thermal annealing in a temperature range of between about 600 and 850 degrees [[C.]] C for a time between about 20 and 60 seconds.

16. (currently amended) The method of claim 13 wherein said first removing said un-reacted salicide material from ~~the surface of~~ said substrate comprises performing a selective wet etch.

17. (currently amended) The method of claim 13 wherein said depositing an isolation film over ~~the surface of~~ said substrate comprises depositing a layer of silicon oxide.

18. (cancelled).

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19. (original) The method of claim 13 wherein said removing said layer of boronitride from said at least one gate electrode comprises applying a Reactive Ion Etch.

20. (currently amended) The method of claim 13 wherein said depositing a thick layer of salicide material over ~~the surface of~~ said polished layer of filler material comprises depositing a layer of Ti/TiN, deposited to a thickness between about 2,000 to 5,000 Angstrom.

21. (currently amended) original) The method of claim 13 wherein said performing a second anneal comprises performing a low temperature anneal performed by rapid thermal annealing in a temperature range of between about 600 and 850 degrees ~~[[C.]]~~ C for a time between about 20 and 60 seconds.

22. (currently amended) The method of claim 13 wherein said second removing un-reacted salicide material from ~~the surface of~~ said layer of filler material comprises performing a selective wet etch.

23. (original) The method of claim 13 wherein said third anneal comprises rapid thermal annealing in a temperature range of

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between about 850 and 1000 degrees C. for a time between about 20 and 60 seconds.

24. (currently amended) A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active ~~surface~~ region as said substrate as defined by regions of Shallow Trench Isolation provided in ~~the surface of~~ the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly ~~[[Doper]]~~ Doped Diffusion regions having been provided in ~~the surface of~~ said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over ~~the surface of~~ said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

depositing a thin layer of Ti/TiN over ~~the surface of~~ said substrate, including ~~the surface of~~ said gate spacers and said layer of polysilicon provided for said at least one gate electrode, deposited to a thickness between about 100 and 500

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~~Angstrom and more preferably to a thickness of about 300~~

~~Angstrom;~~

performing a low temperature anneal of said deposited thin layer of Ti/TiN in a temperature range of between about 600 and 850 degrees ~~[[C.]]~~ C for a time between about 20 and 60 seconds, creating a layer of TiSi_x over ~~the surface of~~ said source and drain implants, leaving uncreated Ti/TiN in place over ~~the surface of~~ said Shallow Trench Isolation regions;

removing said uncreated Ti/TiN from ~~the surface of~~ said substrate by performing a selective wet etch;

depositing a layer of silicon oxide over ~~the surface of~~ said substrate, including ~~the surface of~~ said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of photoresist over ~~the surface of~~ said layer of silicon oxide to a thickness such that ~~the surface of~~ said layer of photoresist extends above ~~the surface of~~ said layer of silicon oxide even where said silicon oxide overlays ~~the surface of~~ said at least one gate electrode;

polishing ~~the surface of~~ said layer photoresist and said layer of silicon oxide down to ~~the surface of~~ said layer of boronitride being part of at least one gate electrode, using

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said layer of boronitride as a stop for said process of polishing;

removing said layer of boronitride from said at least one gate electrode by applying an Reactive Ion Etch, exposing ~~the surface of~~ said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of Ti/TiN over ~~the surface of~~ said polished layer of photoresist, including the exposed surface of said layer of polysilicon, deposited to a thickness between about 2,000 to 5,000 Angstrom[[;]];

performing an anneal of said deposited thick layer of Ti/TiN by rapid thermal annealing in a temperature range of between about 600 and 850 degrees [[C.]] C for a time between about 20 and 60 seconds, creating a layer of TiSi_x overlying said layer of polysilicon of said at least one gate electrode;

removing un-reacted Ti/TiN from ~~the surface of~~ said layer of photoresist by performing a selective wet etch;

performing an anneal of said layer of TiSi_x overlying said layer of polysilicon of said at least one gate electrode, comprising a rapid thermal annealing in a temperature range of between about 850 and 1000 degrees [[C.]] C for a time between about 20 and 60 seconds, reducing [[the]] sheet resistance of

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said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.